ABSTRACT OF THE DISCLOSURE

Methods for improving bus performance and bandwidth utilization in a Local Area Network (LAN) are disclosed along with methods fo adapting LANs for use with differing hardware interfaces. The LANs described are based on a parallel bus architecture. Performance superiority is gained by passing data between ports on parallel circuits that individually are relatively slow, but that, in the aggregate, provide bandwidth equivalent to or greater than serial LAN's of much higher frequency. The bandwidth advantage of the parallel architecture is extended by the logical advantage which permits efficient utilization of up to 99% of this bandwidth. This logical advantage rests in the capability of establishing glare and collision avoidance schemes that result in very little wasted bandwidth. The LANs described are adapted for use with differing hardware interfaces when provided with a plurality of bus ports, where each port has associated therewith a configurable hardware interface.